Andrew V. Podlesny et al. Application No.: 09/505,656

Page 5

## **REMARKS**

Upon entry of this Amendment, which amends claims 1 and 3, cancels claim 2, and adds claims 4-9, claims 1 and 3-9 remain pending.

Claims 1-3 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (U.S. PAT. 5,598,371) in view of Hayakawa (U.S. PAT. 6,184,722 B1).

These rejections are respectfully traversed and reconsideration is respectfully requested on the grounds that the Examiner has not shown claim 1 would have been obvious in view of prior art.

With regard to Lee et al., it is respectfully submitted that Lee et al. teaches a data transfer arrangement comprising two bus drivers and a differential bus coupled to the bus drivers and to the voltage precharge source (PRECH), where the voltage precharge source (PRECH) is coupled to a supply voltage Vcc.

In contrast, the present invention teaches precharging the buses to a specific level between ground and Vdd (Vpr = K\*Vdd, where K is precharging voltage factor), as set out in the specification on page 4, lines 16-30. Precharging the buses to a specific level between ground and Vdd results in equal low differential voltage swings +dV,-Vd, providing increased speed of data transfer, high noise immunity due to the active mode and equal low output resistance of the driver in pull up and pull down modes, and low power consumption by the drivers during the cycle of operation.

Hayakawa teaches a latching sense amplifier coupled to the differential bus.

Applicant respectfully submits that the circuit implementation of the latching sense amplifier in Hayakawa is different from the present embodiment.

The latch-type sense amplifier of the present invention has an output stage to avoid leakage currents and output glitches, which may appear because the potentials of nodes IT and IC are approximately equal to Vpr during the operating cycle of bus driver because the bus driver is precharged to a predetermined level between the ground and the supply voltage. Hayakawa does not teach a latching sense amplifier comprising two stages, where the input of the output stage is coupled to the output of the first stage.



Andrew V. Podlesny et al. Application No.: 09/505,656

Page 6

The sources of cross-coupled latch amplifier NMOS transistors of the Hayakawa latch-type sense amplifier are coupled to the drains of the input pass transistors Q1 and Q2. In the present invention the sources of cross-coupled latch amplifier NMOS transistors are coupled to the drain of NMOS transistor N1, having a gate coupled to the clock signal input. The drains of the input pass transistors are coupled to the drains of the cross-coupled latch amplifier MOS transistors and the input swing passes directly to the high-gain nodes IT and IC of the cross-coupled latched amplifier, providing a higher noise immunity than Hayakawa's.

In the present invention the sources of the PMOS transistors are coupled to the drain of a PMOS transistor having a gate coupled to the inverted clock input, whereas Hayakawa discloses a latch-type sense amplifier with the sources of the PMOS transistors coupled to the supply voltage.

Thus, it is respectfully submitted that none of the prior art, either alone or in combination, discloses, teaches or even suggests the latch-type sense amplifier disclosed in the present invention. Accordingly it is respectfully submitted that claim 1 is allowable.

Claims 3-8 depend, either directly or indirectly on claim 1 and, therefore, they are allowable for at least the reasons claim 1 is allowable. These claims further define and augment the features of applicant's invention.

New independent claim 9 was added. Claim 9 is directed to a method of operation of a data transfer arrangement. The support for claim 9 can be found in Specification on pages 2-5, lines 22-12. As discussed above none of the cited prior art references teach a data transfer arrangement as disclosed in the present invention, and, therefore claim 9 is allowable.

## **CONCLUSION:**

Attached hereto is a marked-up version of the changes made to the claims by the current amendment along with a complete set of claims has been provided for convenience. The attached pages are captioned "Version With Markings To Show Changes Made" and "Claims Appendix."

In view of the foregoing, applicant submits that this application is now in condition for allowance. The issuance of a formal notification to that effect at an early date is requested.



Andrew V. Podlesny et al. Application No.: 09/505,656

Page 7

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

Kevin T. LeMond Reg. No. 35,933

TOWNSEND and TOWNSEND and CREW LLP Two Embarcadero Center, 8<sup>th</sup> Floor San Francisco, California 94111-3834

Tel: Fax: (415) 576-0200 (415) 576-0300

KTL/OV/jtc

SF 1237142 v3

*[*}